MEMORY DEVICE HAVING AN ELECTRON TRAPPING LAYER IN A HIGH-K DIELECTRIC GATE STACK

ABSTRACT OF THE DISCLOSURE

An improved semiconductor memory structure and methods for its fabrication are disclosed. The memory structure includes a semiconductor substrate having a dielectric stack formed over a channel region of a semiconductor substrate. The dielectric stack includes a layer of electron trapping material that operates as a charge storage center for memory devices. A gate electrode is connected with the top of the dielectric stack. In various embodiments the electron trapping material forms a greater or lesser portion of the dielectric stack. The invention includes a method embodiment for forming such a memory device.